

Accelerate your development.

A family of System-on-Modules and development boards



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Products portfolio

TOPIC Embedded Systems (TOPIC) offer a range of embedded solutions that assist developers of complex embedded systems to build their applications quickly, reliably and effectively. Built on AMD System-on-Chip technology, products are available in the form of:

🔺 Miami System-on-Modules (SOMs)

- 🔺 Florida development/carrier boards
- Board support packages based on embedded Linux
- FPGA and processor building blocks in the form of e.g. C/C++ and VHDL code

Supported by our development organisation

A huge benefit of working with TOPIC products is the accessible design support by the TOPIC Projects organization. Apart from in-depth background knowledge of the products, the design teams have significant application development expertise.

Our products are supported by our development organization to help with:

- Design and development services for system engineering and software-, FPGA- and hardware design
- Customization services based on Florida development/carrier boards for rapid prototyping and product development
- Full-custom product development for optimized customer-specific designs
- Application software development (embedded, PCs, cloud, mobile devices)
- Operating System porting as well as BSP/ driver development for e.g. Linux, FreeRTOS and Windows
- Certified development processes for e.g. medical (ISO13485) and safety (CENELEC SIL3/4) projects



Miami System-on-Modules

Technology and concept

The Miami System-on-Modules (SOM) are based on the state-of-the-art silicon technologies of AMD: Zynq 7000, Ultrascale+ and Versal. Their System-on-Chips (SoC) combine processor(s), FPGA logic and accelerators into versatile devices, meeting the latest demanding requirements of applications in medical, industrial, avionics and test and measurement domains. The Miami SOMs enable embedded cutting- edge applications in stand-alone and connected environments. The modules combine high performance and high-density programmable logic with dedicated hardened IP blocks, such as DSP cores, memory controllers, PCIe endpoints and Ethernet MACs. The unique combination of multi-core application processors, real-time processors, optional GPU and AI engines, and feature-rich FPGA fabric makes the Miami a versatile and agile platform for various applications. The multi-gigabit high- speed transceivers enable communication links compatible with different interface standards, such as JESD204, PCIe, SGMII, DisplayPort, SATA, Aurora and SDI.

The Miami SOMs integrate all system components required to bring-up an embedded system including memory, power supplies, debugging facilities and connectivity interfaces at MAC and PHY level. The Miami family of SOMs provide best in class platforms for balancing performance and power consumption, making it a perfect solution for applications that need processing power, high-speed interfaces and have demanding reliability and quality requirements. Key features of the SOM are the ability to optimize system interfaces and component assemblies as well as to execute true real-time arithmetic and control,. The module comes with actively supported board support packages (BSP), including a maintained Linux distribution, supporting the AMD Vitis SDK. All the Miami SOMs are compatible and usable with one of our Florida carrier boards, allowing for rapid prototyping and evaluation purposes.

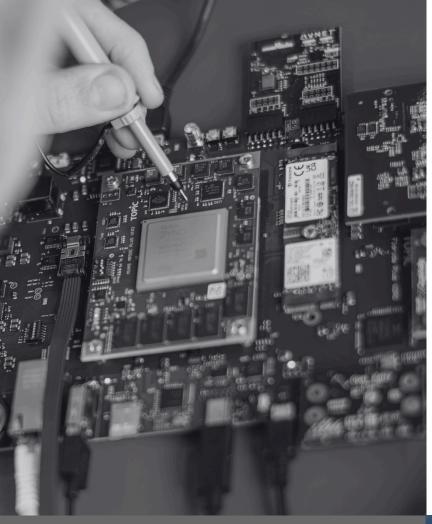
Physical hardware or a SOM-as-IP?

A SOM in the traditional sense is a physical board, integrating the features as described, exposing electrical signals on the connectors towards the mandatory carrier board. The signal assignments, form-factor, pin count and location are all fixed. Occasionally, these constraints are limiting your end-product design. What if you can integrate the SOM circuits, including layer stack-up, placement and routing in your carrier board design and seamlessly fuse your circuits with the SOM-as-IP? All the benefits of a SOM, none of the disadvantages.

The Miami SOM-as-IP is a completely verified and qualified SOM design, available as schematic and PCB design. It has become an integral part of the refence design that you tailor exactly to your needs. There are no connectors to interface with board peripherals and it offers you more flexibility in the board shaping. Never a short of SOC available pins. But most important: the peripheral utilization as well as the signal- and power integrity performance are guaranteed.

The SOM-as-module price is based on the physical variant you need and the volume you buy. The SOM-as-IP pricing is based on a license model. TOPIC Products can support various license models, tailored to your business case. The SOM-as-IP comes with mandatory integration support of our engineering department, covert by the license.





Evaluation and prototyping

Based on the Florida reference designs, customized carrier board variances can be realized reliably, with fast turn-around times. The reference design is available for you as board to start-off already with your prototyping application software and FPGA firmware.

Typical application areas include applications requiring a fair amount of processing power combined with a small system footprint, including but not limited to (secure) communication, high-performance computing, aerospace & defense, audio/video applications, medical, and industrial imaging.

Benefits

- A family of embedded computing solutions, focused on reliability, versatility and certifiability
- Scalable in performance, power, form factor and capabilities
- Based on AMD Zynq 7000, Zynq Ultrascale+ and Versal ACAP System-on-Chip (SOC) technology
- Provides a rich set of state-of-the-art peripherals

Key features

- Small dimensions: <100 mm x <70 mm
- On-board high efficiency power supplies
- Configurable board I/O voltages
- Fast booting capabilities using different processor boot stages and FPGA fabric
- High performance and reliable SAMTEC board-to-board connectors
- On-board DDR3/4 memory with optional ECC support
- Advanced debug support
- Industrial temperature range (-40°C to +85°C)



Miami SOM family in a glance









• AMD SOC technology: Zynq 7000 (7012S, 7015, 7030)

28 nm

55k-125k cells

2x 120 pins

4x GTH (PL)

2016

- Technology node:
- Processors:
- Logic density:
- Connectors:
- Gigabit transceivers:
 - DDR-SDR memory: 1GB 32b DDR3 (PS)
- Introduction date:
- Product details: <u>Miami</u>
- AMD SOC technology: Zynq 7000 (7035, 7045, 7100)
- Technology node: 28 nm
 - Single/dual core ARM Cortex A9

1GB 32b DDR3 (PS), 1GB 32b DDR3 (PL)

Dual/quad core ARM, Cortex A53, Dual core ARM,

Versal Core (VC1502, VC1702, VC1802, VC1902),

Dual core ARM Cortex A72, Dual core ARM Cortex R5F,

Prime (VM1502, VM1802), Edge (VE1752)

2x 120 pins, 1x 180 pins

Single or dual core ARM Cortex A9

- Logic density: 275k-444k cells
- Connectors:

Processors:

- Gigabit transceivers: 16x GTH (PL)
- DDR-SDR memory:
- Introduction date:
- Product details: <u>Miami Plus</u>
- AMD SOC technology: Zynq Ultrascale+ (ZU6, ZU9, ZU15)

2016

- Technology node: 16 nm
- Processors:
- Cortex R7, ARM Mali-400 GPU

2x 120 pins, 1x 180 pins

2GB 72b DDR4 (PS)

AI Engine-ML Tiles

32x GTYP (PL/PS)

Direct PCB interconnect

3x 8/16GB 64b+ECC DDR4 (PL/PS)

3x GTP (PS), 16x GTH (PL)

Logic density: 469k-747k cells

2020

7 nm

Miami Plus

- Connectors:
- Gigabit transceivers:
- DDR-SDR memory:
- Introduction date:
- Product details:

AMDA AMDA

Al Core
 Al Core
 AMD SOC technology:

- Technology node:
- Processors:
- Logic density: 981k 1968k cells
- Connectors:
- Gigabit transceivers:
- DDR-SDR memory:
 - Introduction date: Under development
 - Product details: <u>Miami Ultra</u>



Florida carrier boards

Benefits

- Evaluation boards for the Miami System-on-Modules
- Development platform for kick-starting a design
- Reference designs, schematics and printed circuit board layouts available
- Customize the board to your own needs or make use of our fast-turn-around board customization services

Key features

- Gigabit transceiver support for PCI Express, SATA, Aurora
- Ethernet LAN interface
- Display interfaces
- Opal Kelly SYZYGY compliant interfaces
- Digilent PMOD compliant interfaces
- FMC compliant interfaces
- Bluetooth, WiFi, mass-storage
- USB-C, 3.0 and 2.0 OTG
- UART via USB

Evaluation and prototyping



The Florida carrier boards are designed to evaluate the capabilities of the AMD Zynq[®] or Zynq Ultrascale+[®] based Miami Systemon-Modules (SoM) and provide a means for rapid prototyping. The boards offer a rich pool of peripherals. Together with an accessories bag, a Florida carrier board and Miami SoM of choice form a complete development platform. The kit configuration helps kick-starting your application development in an early stage, giving access to the complete feature set of the processing system using the provided reference design and Linux board support package (BSP).

The interfaces on the carrier boards provide functionality to support data acquisition, visualization, human-machine interfaces, and communication. With a Florida platform, an application can be prototyped and validated. Software and FPGA reference designs, schematics and printed circuit board layout are available as a starting point for a dedicated carrier board design. The functions on the carrier boards are validated in different applications, guaranteeing high quality circuitry. TOPIC also offers driver development support as a service. The same is applicable for the carrier board customization: TOPIC offers board design and production services to facilitate quick and reliable hardware realization.

Florida carrier boards are off-the-shelf available in a number of configurations. Each Florida supports a specific Miami SoM. The carrier boards differ in supported peripherals and evaluation context. The peripherals supported meet the capabilities of the processing system as well as the intended use cases of the FPGA fabric and other SoC features. The Florida Plus supports the latest generation peripherals and communication interfaces, for the Miami MPSOC Plus capabilities.

Peripheral diversity

Given the flexibility of the connectors and interfaces on the carrier boards, a variety of functionality is made available: SATA, M.2 based PCIe, Gigabit Ethernet, SDIO/SDcard interface, FMC and PMOD Generic I/O expansion ports, DisplayPort/HDMI/DVI/MIPI video capture and generation, virtual COM ports, JTAG debug ports, LEDs and switches. This makes it possible to prototype a complete instrument containing visualization, communication, control, and data storage/offloading.

Customization services

Customized application

TOPIC offers Florida carrier board customization services to rapidly create a custom carrierboard according to specific requirements with short times and optionally succeeded by the production and assembly of the boards. Peripherals used on the evaluation boards are applied in various applications, resulting in robust circuit design, thorough testing, extensive software support and compliant (EMC) qualification. Customization can be supported by our board- and reference designs. The carrier board schematics and board layout files are available as inspiration and under certain conditions as Mentor Graphics or Altium design files.

TOPIC can customize a carrier board according to specific needs. As an experienced product development organization, we design and manufacture customized boards according to the requirements we agreed upon, as well as test and qualification criteria that are applicable. As the Miami SoMs are qualified according to industrial design constraints, TOPIC customized carrier boards can comply to these same constraints when required.

Prototype production of the carrier boards is always carried-out under the responsibility of TOPIC as this is part of the qualification process. Thereafter, the choice of production partner is open. Feel free to contact TOPIC to discuss the possibilities.

Benefits

- The development services provided by TOPIC are flexible and customer specific
- Customization services are available for board design, software development and FPGA design
- Application software development based on e.g. Qt, OpenCV, Python, Docker, ROS, .NET
- Operating System porting as well as (Linux) BSP/ driver development and support
- RAMS (Reliability, Availability, Maintainability, Safety) aware development
- Development processes executed according to e.g. IEC60601, ISO13485 and ISO14971 standards.



About TOPIC Embedded Systems

"We make the world a little better, healthier and smarter every day". Our mission statement reflects exactly what we do: developing innovative systems for our customers. The way we do that, is by combining our customers domain specific know-how with our expertise in hardware and software development. This results in the most optimal product for our customers. TOPIC has a strong background of more than 27 years in developing systems, which can contain embedded-, application- and cloud software, FPGA code and PCB designs. We help customers in different domains such as medical, imaging, machine control & safety. With over 130 employees, we are a strong and established company with our headquarters in Best, the Netherlands. TOPIC has an ISO13485 (medical) certified Quality Management System and adopted the Agile way-of-working for optimal interaction with the customer.

Premier Partnership with AMD | TOPIC is one of the few AMD Premier Adaptive Computing partners in the world. Our partnership started in 2009 and since than we have been working closely together over the last years.

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Product details Miami

Miami type	Miami	Miami	Miami			
AMD SOC Technology						
Order number FPGA	mia-7z12-1-2-3	mia-7z15-1-2-3	mia-7z30-1-2-3			
	XC770125 CLC 495 1	XC7701E CL C 49E 1	VC77020 CDC 495 1			
Device*	XC7Z012S-CLG485-1	XC7Z015-CLG485-1	XC7Z030-SBG485-1			
Technology	Artix®-7	Artix®-7	Kintex®-7			
.ogic cells	55K	74K	125K			
Flip Flops	68,8	92,4	157,2			
Block RAM	320KB	380KB	1.060MB			
JltraRAM	-	-	-			
DSP slices	120	160	400			
GTx (PL controlled)	4x (3.75Gb/s each)	4x (3.75Gb/s each)	4x (6.6 Gb/s each)			
Processor System		(
Application Processor (cores)	ARM Cortex-A9 (single)	ARM Cortex-A9 (dual)	ARM Cortex-A9 (dual)			
CPU Performance	666MHz	666MHz	800MHz			
Co-Processor	1x ARM NEON tm	2x ARM NEON tm	2x ARM NEON tm			
Real-Time Processor (cores)		-	-			
1.264/H.265 Video Codec	-	-	-			
Al Engine-ML Tiles	-	-	-			
Vetwork-on-Chip M/S ports	-		-			
Graphics Processor	-	-	-			
GTx (PS controlled)	-	-	-			
Memory						
	11.2000	instruction/coro 20KP data/an	2 1 2· 512KP			
Cache (application processor)	L 1: 32KB	instruction/core, 32KB data/core	S, LZ: DIZNB			
Cache (real-time processor)		-				
Cache (GPU)		-				
DRAM (PS/PL controlled)	DDR3/DDR3L @ 533MHz, 1 GB					
DRAM (PL only controlled)		-				
NOR		Quad-speed SPI, 32MB				
NAND						
EPROM	4	- Khaanfiguration/naromatorata				
	4	Kb configuration/parameter sto	rage			
User programmable/configurable interfaces						
PS connected I/O		26x PS controlled 1V8 I/O (MIC				
PL connected HD I/O	49x programmable user I/O (HR)					
PL connected HP I/O	47	x + 45x programmable user I/O	(HP)			
Safety and security						
Supported safety standards	ISO26262 IEC	C61508, IEC62061, ISO 13849, D0	0-254/D0178b			
Certification support	10020202,12					
	AMD functional safety package					
Security support	Anti-tempering, cyber-security, embedded encryption, secure-boot, isolation					
Time synchronisation	Precision tir	ning (IEEE 1588 HA), White Rabb	Dit, SyncE, PTP			
Dedicated interfaces on SoM connector						
Network		2x 10/100/1000 Mbps Etherne	t			
JSB	2x USB OTG 2.0					
PS peripherals	2x CAN (ISO 11		DIO, 2x I2C. 2x SPI			
Gigabit transceivers	2x CAN (ISO 11898-1, 2.0A, 2.0B), 2x UART, 2x SDIO, 2x I2C, 2x SPI					
PCI-Express (end-point/root-complex)	SATA-2/3, PCIe GEN2 4 lanes, Aurora, CoaXPress, HDMI, USB 3.0					
	GEN2 - 4 lanes					
GTx (PS controlled)		-				
GTx (PL controlled)		, PCIe GEN3, 40Gb Ethernet, Co				
Miscellaneous	GPIOs, SD/SDIO 2.0/MMC 3.31 compliant controllers					
ITAG	PL JTAG chain for carrier board programming					
Debug	Debug UART, console					
5		Debug OART, console				
Supply	0.01////					
Power supply input		board voltage regulation, curren				
ogic I/O supply output	Cor	figurable I/O standards and vol	tages			
Software support						
Bootloader / BSP		U-Boot				
Boot resources	1.	TAG, NOR, (carrier board) SD-C	ard			
Operating System						
	Yocto/PetaLinux managed Linux kernel/BSP					
PGA reference design	Vivado BSP and module configuration					
Carrier board (order number)		Florida Gen (flo-gen)				
Mechanical and environmental						
Dimensions		65mm x 68.4mm				
Connectors	2x 120 pin Samtec high performance mezzanine carrier board connectors					
Comporatura	los	ustrial graded IEC 60068-2-29.	2009			
lemperature	Industrial graded, IEC 60068-2-38:2009					
Temperature and humidity	0%-95%, non-condensing, IEC 60068-2-38:2009					
EMC/EMI	EN 55032 / IEC 61132, EN 61326, IEC 55024					
Shock and vibration		(method 204D), MIL-STD-202F	1 101003			

Product details Miami Plus

Miami type	Miami Plus	Miami Plus	Miami Plus			
AMD SOC Technology						
Order number	miap-7z35-2-2-3	miap-7z45-2-2-3	miap-7z100-2-2-3			
FPGA						
Device*	XC7Z035-FFG900-2	XC7Z045-FFG900-2	XC7Z100-FFG900-2			
Technology	Kintex [®] -7	Kintex®-7	Kintex®-7			
Logic cells	275K	350K	444K			
Flip Flops	343,8	437,2	554,8			
Block RAM	17,6	19,1	26,5			
JltraRAM	-	-	-			
DSP slices	900	900	2020			
GTx (PL controlled)	16x (10.3125 Gb/s each)	16x (10.3125 Gb/s each)	16x (10.3125 Gb/s each)			
Processor System						
Application Processor (cores)	ARM Cortex-A9 (dual)	ARM Cortex-A9 (dual)	ARM Cortex-A9 (dual			
CPU Performance	2x 800MHz	2x 800MHz	2x 800MHz			
Co-Processor	2x ARM NEON tm	2x ARM NEON™	2x ARM NEON tm			
Real-Time Processor (cores)	-	-	-			
H.264/H.265 Video Codec	-	-	-			
Al Engine-ML Tiles	-	-				
Network-on-Chip M/S ports		-				
Graphics Processor		-				
GTx (PS controlled)	-	-				
Memory	-					
	1.1.20KD :	truction (see 22KD date (see 1	2. 512KD			
Cache (application processor)	L1: 32KB ins	struction/core, 32KB data/core, l	Z. JIZND			
Cache (real-time processor)		-				
Cache (GPU)		•				
SDRAM (PS/PL controlled)		DDR3/DDR3L @ 533MHz, 1 GB				
SDRAM (PL only controlled)	[DDR3/DDR3L @ 533MHz, 1 GB				
NOR		2x Quad-speed SPI, 64MB				
NAND		-				
EEPROM	4 Kb	o configuration/parameter storage	ge			
User programmable/configurable interfaces						
PS connected I/O	49x + 47 + 48 (Configurable 1V8, 2V5 and 3V3	user I/O (HR)			
PL connected HD I/O	48x Configurable 1V8 user I/O (HP)					
PL connected HP I/O		8x PS controlled 1V8 I/O (MIO)				
Safety and security						
Supported safety standards	ISO26262, IEC6	1508, IEC62061, ISO13849, DO-	254/DO178b			
Certification support		AMD functional safety package				
Security support	AMD functional safety package Anti-tempering, cyber-security, embedded encryption, secure-boot, isolation					
Time synchronisation		ng (IEEE 1588 HA), White Rabbit				
Dedicated interfaces on SoM connector	r recision ann	ing (IEEE 1000 I A), white habble	, Synce, I m			
Network		2x 10/100/1000Mbpc Ethorpot				
USB	2x 10/100/1000Mbps Ethernet					
	2x USB OTG 2.0					
PS peripherals	2x CAN (ISO 11898-1, 2.0A, 2.0B), 2x UART, 2x SDIO, 2x I2C, 2x SPI					
Gigabit transceivers	SATA-3, PCIe GE	EN2 8 lanes, Aurora, CoaXPress, I	IDIVII, USB 3.0			
PCI-Express (end-point/root-complex)		GEN2 - 8 lanes				
GTx (PS controlled)		-				
GTx(PL controlled)		PCIe GEN3, 40Gb Ethernet, Coa				
Miscellaneous	GPIOs, SD/SDIO 2.0/MMC 3.31 compliant controllers					
JTAG	PL and PS JTAG chain for shared debugging					
Debug	Debug UART, console					
Supply						
Power supply input		15V/3A				
Logic I/O supply output	Confi	gurable I/O standards and volta	aes			
Software support	Conn	galasie i e standurds und volta	3			
Bootloader / BSP		U-Boot				
Boot resources	IT A	AG, NOR, (carrier board) SD-Car	4			
Operating System	Yocto/PetaLinux managed Linux kernel/BSP					
FPGA reference design	Viva	do BSP and module configuration	011			
Carrier board (order number)		Florida Test (flo-test)	1			
Mechanical and environmental						
Dimensions		85mm x 68.5mm				
Connectors	2x 120 pins + 1x 180 pins Samtec high performance mezzanine carrier board connectors + 1x 3 pin fan connector					
Tana a satura	mezzanine carr		anconnector			
Temperature	Industrial grade					
Temperature and humidity	IEC 60068-2-1 (Cold), IEC 60068-2-2 (Dry heat), IEC 60068-2-78 (Damp heat)					
EMC/EMI	EN 55032, IEC 61132, EN 61326, IEC 55024					
Shock and vibration	MIL_STD_202G (method 204D), MIL-STD-202G (method 213B)			

Product details Miami Plus

Miami type	Miami Plus	Miami Plus	Miami Plus		
AMD SOC Technology					
Order number	miap-zu6-1-6-4-2	miap-zu9-1-6-4-2	miap-zu15-1-6-4-2		
FPGA					
Device*	XCZU6-EG-1FFVB1156I	XCZU9-EG-1FFVB1156I	XCZU15-EG-1FFVB1156I		
「echnology	Ultrascale+®	Ultrascale+®	Ultrascale+®		
_ogic cells	469K	600K	747K		
Flip Flops	429K	548K	682K		
Block RAM	25.1Mbit	32.1Mbit	26.2Mbit		
JItraRAM	-	-	31.5Mbit		
DSP slices	1973	2520	3528		
GTx (PL controlled)	16x (12.5 Gbit/s each)	16x (12.5 Gbit/s each)	16x (12.5 Gbit/s each)		
	Tox (12.5 Gbit/s each)	Tox (12.5 Gbit/s each)	Tox (12.5 Gbit/s each)		
Processor System			1014.0		
Application Processor (cores)	ARM Cortex-A53 (quad) ARM Cortex-A53 (quad)		ARM Cortex-A53 (quad)		
CPU Performance	4x 1.2GHz	4x 1.2GHz	4x 1.2GHz		
Co-Processor	4x ARM NEON™	4x ARM NEON™	4x ARM NEON™		
Real-Time Processor (cores)	ARM Cortex R5 (dual)	ARM Cortex R5 (dual)	ARM Cortex R5 (dual)		
H.264/H.265 Video Codec	-	-	-		
Al Engine-ML Tiles	-	-			
Network-on-Chip M/S ports					
Graphics Processor	- ARM Mali™-400 MP2	- ARM Mali™-400 MP2	- ARM Mali™-400 MP2		
GTx (PS controlled)	3x (6 Gbit/s each)	3x (6 Gbit/s each)	3x (6 Gbit/s each)		
Memory					
Cache (application processor)		D per core, L2: 1MB, on chip me			
Cache (real-time processor)	L1: 32KB I / D p	er core, tightly coupled memory	128 KByte per core		
Cache (GPU)		64 Kbyte			
SDRAM (PS/PL controlled)	2.4 or 8 GBvte DDR4	with/without ECC (assembly option	on 32, 64 or 72 bits wide)		
SDRAM (PL only controlled)	2,1010 00 910 00 111				
NOR	Quada	peed SPI, (64 MByte, 128 MByte,	254 MP: to)		
NAND	0, 8,	16, 32 or 64 GByte pseudo-SLC			
EEPROM		32 Kbit I2C EEPROM storage			
User programmable/configurable interfaces					
PS connected I/O	DC compact				
3 connected 1/O	rs connec	ted 1.8V GPIO, multiplexed peri	pherals (MIO)		
PL connected HD I/O		ted 1.8V GPIO, multiplexed peri nm impedance controlled and le			
PL connected HD I/O PL connected HP I/O					
PL connected HD I/O PL connected HP I/O Safety and security	HP and HD GPIO, 100 OI	nm impedance controlled and le	ngth matched within quads		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards	HP and HD GPIO, 100 OI	nm impedance controlled and le C61508, IEC62061, ISO13849, D	o-254/DO178b		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support	HP and HD GPIO, 100 OI ISO26262, IE	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag	o-254/DO178b		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybe	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag er-security, embedded encryptic	ongth matched within quads O-254/DO178b e on, secure-boot, isolation		
PL connected HD I/O PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Time synchronisation	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybe	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag	ongth matched within quads O-254/DO178b e on, secure-boot, isolation		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Fime synchronisation	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybe	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag er-security, embedded encryptic	ongth matched within quads O-254/DO178b e on, secure-boot, isolation		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Fime synchronisation Dedicated interfaces on SoM connector	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybe Precision ti	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag er-security, embedded encryptic ming (IEEE 1588 HA), White Rab	ongth matched within quads O-254/DO178b e on, secure-boot, isolation bit, SyncE, PTP		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Fime synchronisation Dedicated interfaces on SoM connector Network	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybo Precision ti 10/100/1000Mbps	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag er-security, embedded encryptic ming (IEEE 1588 HA), White Rab Ethernet, (PHY included), IEEE 15	O-254/DO178b e on, secure-boot, isolation bit, SyncE, PTP 588 and SyncE support		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Fime synchronisation Dedicated interfaces on SoM connector Network JSB	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybo Precision ti 10/100/1000Mbps 10G/	nm impedance controlled and le C61508, IEC62061, ISO13849, D AMD functional safety packag er-security, embedded encryptic ming (IEEE 1588 HA), White Rab Ethernet, (PHY included), IEEE 15 40G/50G support (external PHY	ongth matched within quads O-254/DO178b e on, secure-boot, isolation bit, SyncE, PTP 588 and SyncE support needed)		
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PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Time synchronisation Dedicated interfaces on SoM connector Network USB PS peripherals Gigabit transceivers PCI-Express (end-point/root-complex) GTx (PS controlled) GTx (PC controlled) Miscellaneous JTAG Debug Supply Power supply input Logic I/O supply output Software support Bootloader / BSP Boot resources Operating System FPGA reference design Carrier board (order number) Mechanical and environmental Dimensions Connectors	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybo Precision ti 10/100/1000Mbps 10G/ CAN (IS e.g. FPI 2x L 3x (ć 16x (PCle GEN3/4, 4 GPIOs, S PL an Debug 9.0- 16.0 Vdc via carrier bo Selectab	am impedance controlled and le C61508, IEC62061, ISO13849, Dr AMD functional safety packag er-security, embedded encryptic ming (IEEE 1588 HA), White Rab Ethernet, (PHY included), IEEE 15 40G/50G support (external PHY 40G/50G support (external PHY 0 11898-1, 2.0A, 2.0B), UART, SD 0 11898-1, 2.0A, 2.0B, 2.0A, 2.0B), UART, SD 0 11892-1, 2.0A, 2.0B, 2.0A, 2.	ormance		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support Time synchronisation Dedicated interfaces on SoM connector Network USB PS peripherals Gigabit transceivers PCI-Express (end-point/root-complex) GTx (PL controlled) Miscellaneous JTAG Debug Supply Power supply input Logic I/O supply output Software support Boot resources Operating System PFGA reference design Carrier board (order number) Mechanical and environmental Dimensions Connectors	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybo Precision ti 10/100/1000Mbps 10G/ CAN (IS e.g. FPI 2x L 3x (6 16x (PCle GEN3/4, 4 GPIOs, S PL an Debug 9.0- 16.0 Vdc via carrier bo Selectat	am impedance controlled and le C61508, IEC62061, ISO13849, Dr AMD functional safety packag er-security, embedded encryptic ming (IEEE 1588 HA), White Rab Ethernet, (PHY included), IEEE 15 40G/50G support (external PHY 40G/50G support (external PHY 10G/50G support (external PHY 10G/50G support, external PHY 10G/50G support, extern	ormance in fan connector		
PL connected HD I/O PL connected HP I/O Safety and security Supported safety standards Certification support Security support	HP and HD GPIO, 100 OI ISO26262, IE Anti-tempering, cybo Precision ti 10/100/1000Mbps 10G/ CAN (IS e.g. FPI 2x L 3x (6 16x (PCle GEN3/4, 4 GPIOs, S PL ar Debug 9.0- 16.0 Vdc via carrier bo Selectat JT 2x 12 mezzanine c IEC 60068-2-1 (Cold	am impedance controlled and le C61508, IEC62061, ISO13849, Dr AMD functional safety packag er-security, embedded encryptic ming (IEEE 1588 HA), White Rab Ethernet, (PHY included), IEEE 15 40G/50G support (external PHY 40G/50G support (external PHY 0 11898-1, 2.0A, 2.0B), UART, SE D link, SDI, TFT, HDMI (PL), Displ SB 3.0, including on-board ULPI Gbit/s each, DisplayPort, PCIe, U 40Gb Ethernet, USB 3.0, CoaXPre D/SDIO 2.0/MMC 3.31 complian nd PS JTAG chain for shared deb g UART, console, PS JTAG, PL JTA ard connector, 50[W] maximum. ble I/O standards and voltages fo U-Boot / Linux AG, QSPI-NOR, eMMC, SD-Card Topic Linux distribution on GitH Florida Plus (flo-plus) 95mm x 68.5mm 10 + 1x 180 pin Samtec high perf arrier board connectors + 1x 3 p	ormance in fan connector 0068-2-78 (Damp heat)		

Product details Miami Ultra (as IP)

Miami type		Miami Ultra			Miami Ultra	Miami Ultra	
AMD SOC Technology							
Order number	miav-ip-vc1902	miav-ip-vc1902 miav-ip-vc1802 miav-ip-vc1702 miav-ip-vc150		miav-ip-vc1502	miav-ip-ve1752	miav-ip-vm1802	miav-ip-vm150
FPGA							
Device*	X	XCVC1 [9/8/7/5] 02-1MSEVSA2197 Versal® AI Core			XCVE1752-1MSEVSA2197 XCVM1[8/5]802-1MSEVSA21		
Technology	10494			10224	Versal® Al Edge 981K	Versal® Al Prime	
Logic cells Flip Flops	1968K	1600K	1312K	1032K	901K	1968K	981K
Block RAM	24545.3	20141-14	24446.14	20146.14	24146.14	24141-3	34Mbit
UltraRAM	34Mbit	28Mbit 91Mbit	34Mbit	30Mbit	34Mbit	34Mbit	
	130Mbit		130Mbit	130Mbit	130Mbit	130Mbit	130Mbit
DSP slices	1968	1600	1312	1032	1312	1968	1312
GTx (PL controlled)			VC1502: 32	GIY, all others: 4	4x GTY (32 Gbit/s each)		
Processor System				APM Contox A	72 (dual)		
Application Processor (cores) CPU Performance		ARM Cortex-A72 (dual) 2x 1.5GHz					
Co-Processor				2x 1.5G			
Real-Time Processor (cores)				ARM Cortex R	or (dual)		
H.264/H.265 Video Codec	100	200	204	-	204	1	
Al Engine-ML Tiles	400	300	304	198	304	-	-
Network-on-Chip M/S ports	28	28	21	21	21	28	21
Graphics Processor				-			
GTx (PS controlled)				-			
Memory			11.20/01/0	ar aars 1.0.4145	on ohin man an OF (KD)		
Cache (application processor)		L1: 32KB I/D per core, L2: 1MB, on chip memory 256 KByte					
Cache (real-time processor)		L1: 32KB I/D per core, tightly coupled memory 128 KByte per core					
Cache (GPU)		· ·					
SDRAM (PS/PL controlled)							
SDRAM (PL only controlled)		3x, 8 or 16 GByte LPDDR4 with/without ECC (assembly option) 64 or 72 bits wide)					
NOR		Quad/octal-speed SPI, (128 MByte, 256 MByte)					
NAND		0, 16, 32, 64 or 128 GByte pseudo-SLC or MLC eMMC					
EEPROM				64 Kbit I2C EEPR	OM storage		
User programmable/configurable interfa	aces						
PS connected I/O					plexed peripherals (MIO)		
PL connected HD I/O				~	atched within SelectIO ban		
PL connected HP I/O		100 Ohm in	npedance contro	lled and length n	natched within SelectIO ban	iks, 1V5 max.	
Safety and security			1000101010				
Supported safety standards					013849, DO-254/DO178b		
Certification support					e, board pre-qualification		
Security support		Anti-te	1 0.1		ed encryption, secure-boot, i	isolation	
Time synchronisation			Precision timir	ng (IEEE 1588 HA)	, White Rabbit, SyncE, PTP		
Dedicated interfaces on SoM connector							
Network		10	/100/1G/2.5G/10		s Ethernet, IEEE 1588v2 supp	port	
USB		2x USB 3.0					
PS peripherals		UART, I2C, SPI, I2S, CAN (user configurable/selectable)					
Gigabit transceivers		e.g. FPD link, SDI, TFT, HDMI (PL), DisplayPort (PS), Ethernet, ADC/DAC					
PCI-Express (end-point/root-complex)				1x GEN4x16, 4	GEN4x8		
GTx (PS controlled)				-			
GTx (PL controlled)		16x (PC			ess, HDMI, DisplayPort, JESD	204B/C)	
Miscellaneous					31 compliant controllers		
JTAG		PL and PS JTAG chain for shared debugging, ARM Core Connect support					
Debug			Debug U	ART, console, PS J	TAG, PL JTAG, 4 pins		
Supply							
Power supply input		42-54 Vdc via carrier board connector, 100[W] maximum. On-board voltage regulation.					
Logic I/O supply output		Selectable I/O standards and voltages for					
Software support							
Bootloader / BSP				U-Boo			
Boot resources		JTAG, NOR, SD-Card					
Operating System		Topic Linux distribution on GitHub, AMD Vitis reference design					
FPGA reference design		Vivado reference design and module configuration					
Carrier board (order number)				Florida Ultra (ílo_ultra)		
Mechanical and environmental							
Dimensions				80mm x 8	Omm		
Connectors		Not applicable. Wiring stubs on defined edges of the IP block					
Temperature			Industrial grad	e (extended tem	perature range on request)		
Temperature and humidity		IEC 60	-		heat), IEC 60068-2-78 (Dam	np heat)	
EMC/EMI					V 61326, IEC 55024		
Shock and vibration					L-STD-202G (method 213B)	



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