

Monday, December 25, 2017

Our Ref: QD_LA_2017_12_25

Subject: Field Oriented Control Library and Motor Control Intellectual Property (IP) cores evaluation license.

Product ID: FOCLIB_EVAL_V_1.0

GLOSSARY

| | |
|-------|-------------------------------------|
| FPGA | Field Programmable Gate Array |
| FOC | Field Oriented Control |
| IP | Intellectual Property |
| PI | Proportional Integral control |
| VHDL | VHSIC Hardware Description Language |
| VHSIC | Very High Speed Integrated Circuits |

Dear Sirs:

QDESYS is glad to license the FOCLIB_EVAL_V_1.0 listed in the Table IP DESCRIPTION and the associated documentation.

The Licensed Material is identified in the next Table as High Performance Field Oriented Control IP and listed in the Table IP DESCRIPTION.

The licensed Material usage is limited to evaluation, and hobbyist non -commercial usage only.

The Reference Designs, Application Note, Microblaze Network Agent C source code and GUI Graphical User Interface are provided 'AS IS' as complimentary with no warranty.:

| PROVIDED WITH CORES | | |
|---|--------------------------|---|
| ITEM | FORMAT | DESCRIPTION |
| High Performance Field Oriented Control IP | FPGA IP CORES | total of 18 IP |
| Documentation | Data Sheets | total of 18 data sheets |
| Design File Formats | Encrypted VHDL (1) | See list of IP included |
| Constraint Files | Xdc | 1 |
| Instantiation Templates | VHDL | 1 |
| Reference Designs & Application Notes | Vivado sample design | 1 |
| Microblaze Network Agent C source code | C | |
| GUI Graphical User Interface | Executable Windows-10x64 | Requires .NET (free), NI - Labstudio (free) |

The offered Package is compatible with **Xilinx Vivado 2017.4**

The offered product is compatible with the following Xilinx™ FPGA families:

- Zynq- 7000
- KINTEX- 7®.

The offered products can be evaluated and applications developed on the following platforms

| PLATFORMS | | | |
|----------------------------------|-------------------|-----------------------|--------|
| Platform Zynq-7000 EPP ZC702 Kit | EK-Z7-ZC702-CES-G | XC7Z020 CLG484 -1 EPP | Xilinx |
| ZedBoard™ Zynq-7000 | AES-Z7EV-7Z020-G | XC7Z020 CLG484 -1 EPP | Avnet |
| Trenz Electronic Zynq-7000 | TE0720/TE0701 | XC7Z020-2CLG484I | Trenz |

The Package contains the following IPs.

| IP DESCRIPTION | |
|--|----------------|
| Encoder | encdig3w.vhd |
| Rotor electrical angle emulator | manrot.vhd |
| Clarke's transformation | clarke.vhd |
| Park and inverse Park transformation | park.vhd |
| Low pass filter of first order | filtrir.vhd |
| Multi-functional Space Vector PWM modulator | pwmmod.vhd |
| Initialized double port BRAM 1024x18 wrapper | bram1k18.vhd |
| Interpolated Sine and cosine functions | sincos.vhd |
| Arcotangent2 function | atan2.vhd |
| Flexible Integer division with remainder | idivision.vhd |
| PI regulator with anti-windup | pi_control.vhd |
| Cartesian to polar coordinates conversion | rectopol.vhd |
| Recursive Pulse Frequency Modulator | rpfm.vhd |
| Dynamic Offset Tuner | adjadval.vhd |
| RPFM space vector modulator | Rpfm3phmod.vhd |
| Sliding Mode observer | Posslmeval.vhd |
| Hall sensors position evaluation | Hallsnsp.vhd |
| FOC module | motorfoc.vhd |

FOC module contains all the listed IP.

The Package includes:

- GUI (Graphic User Interface)
- Scripting DLL
- Datasheets and examples
- 8 hours of phone assistance

Training can be provided with separate offer

Service and Integration can be provided with separate offer

Sincerely,

Diego Quagreda

QDESYS LICENSE AGREEMENT

Licensee:

Licensee address:

Licensee's authorized representative:

Effective Date:

December 25, 2017 _____

Authorized Site: The company address

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 - b. To perform in the manner and under the conditions as specified in Seller's warranty for the individual Product or for twelve (12) months from shipment if a warranty for an individual product is not specified.
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- e. Non conformity is the discrepancy between the intended behavior described in the IP datasheet and the actual behavior. In case of non conformity QDESYS reserves the right to update the documentation or correct the IP behavior if QDESYS recognizes the non conformity as defect.
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- i. A precondition for all claims against QDESYS shall be that the defect is reproducible or can be displayed through mechanically generated copies.
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